## REMARKS

This Supplemental Amendment is being filed subsequent to the Amendment accompanying a Request for Continued Examination (RCE) filed on April 14, 2005, and is proper under 37 C.F.R. § 1.111(a)(2) because it simplifies the issues for appeal.

In this Supplemental Amendment, Applicants have amended claim 28. Claims 27, 28, and 30 to 33 are pending in the above-captioned patent application.

In the final Office Action, the Examiner rejected claims 27, 28, and 30 to 33 under 35 U.S.C. § 102(b), as being anticipated by U.S. Patent No. 5,188,976 ("Kume et al.")

Applicants continue to traverse the Examiner's rejection for reasons discussed in the Amendment dated April 14, 2005.

Applicants discussed the Examiner's rejection during an interview on May 5, 2005. Applicants appreciate the courtesy extended by the Examiner in granting the interview.

During the interview, Applicants addressed the Examiner's assertion that Fig. 15 of Kume et al. shows that "side wall of first gate electrode 17 [in the] (memory area) is connected to side wall of second gate 17 [in the] (first peripheral area)." See Final Office Action at 3. The Examiner agreed that Fig. 15 as well as Fig. 14 of Kume et al. failed to show the sidewall of a gate electrode in the memory area being connected to the sidewall of a gate electrode in the first peripheral transistor area, as alleged in the Final Office Action. The Examiner nevertheless asserted that Kume et al.'s Fig. 14 illustrates a portion of conductive film 17 in the first peripheral area (allegedly corresponding to the first gate electrode) and a portion of conductive film 17 in the

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second peripheral area (allegedly corresponding to the second gate electrode) are connected.

Applicants respectfully disagree with the Examiner's interpretation of Fig. 14.

Specifically, Fig. 14 of <u>Kume et al.</u> shows only one <u>continuous</u> conductive film 17, covering both the first and the second peripheral transistor areas. Therefore, Fig. 14 clearly does not show the claimed first <u>and</u> second gate electrodes.

Moreover, Applicants note that claim 27 recites <u>first and second transistors</u> including first and second gate electrodes, respectively. In contrast, in the intermediate process steps shown Figs. 14 and 15, for example, film 17 is just that, a film. Film 17 is <u>not</u> a gate electrode in either Fig. 14 or Fig. 15 because it is not part of a completed transistor. Accordingly, for this reason also, <u>Kume et al.</u>'s Figs. 14 and 15, as well as other cited portions of the reference, fail to teach the claimed first and second gate electrodes.

Only Figs. 18, 22 and 28 of Kume et al. show completed devices, which include transistors. However, each of these figures clearly shows that the sidewalls of each gate electrode in its respective transistor area, such as the side wall of gate electrode 40 in Fig. 18, the side wall of gate electrode 17 in Fig. 22 and the side wall of gate electrode 49 in Fig. 28, are covered by side wall spacers 26 and insulating film 33. Thus, according to Kume et al., the sidewalls of the gate electrodes in the transistors are certainly not connected as claimed. Rather, Kume et al. teaches away from the claimed "side wall of the first gate electrode... connected to a side wall of the second gate electrode."

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In light of the above-described deficiencies of <u>Kume et al.</u>, Applicants respectfully submit that claim 27 is allowable over <u>Kume et al.</u> because it at least fails to teach the claimed "side wall of the first gate electrode is connected to a side wall of the second gate electrode." Moreover, claims 28 and 30 to 33 are allowable at least due to their dependency from claim 27.

Also during the interview, the Examiner indicated that the term "perpendicular" in claim 28 is the same as the phrase "when viewed from a direction <u>perpendicular</u> to the first direction" in claim 27.

Applicants respectfully point out that the term "perpendicular" was used in claim 27 to indicate a cross-sectional direction. On the other hand, the term "perpendicular" was used in claim 28 to describe the <u>vertical orientation</u> of claim 33's "side insulator film formed on a side wall of the second insulation film and a side wall of the polysilicon layer". <u>See also</u> Fig. 13D of the specification.

While Applicants disagree with the Examiner's interpretation of the term "perpendicular" in claim 28, Applicants have amended claim 28 to further clarify the claimed "side insulator film formed on a side wall of the second insulation film and a side wall of the polysilicon layer." Support for the amendments to claim 28 can be found at least in the specification, for example, at Figure 13D, and page 36, lines 10 to 15 of the specification. Therefore, amended claim 28 is further distinguishable over <a href="Kume et al.">Kume et al.</a> does not teach "a side of the side insulator film is on a surface of said semiconductor substrate" as claimed.

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In view of the foregoing remarks, and for the reasons set forth in Applicants' April 14, 2005, Amendment, Applicants respectfully request the reconsideration of the present application and the timely allowance of pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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